ISL/L00 VRB Load Balancing Update

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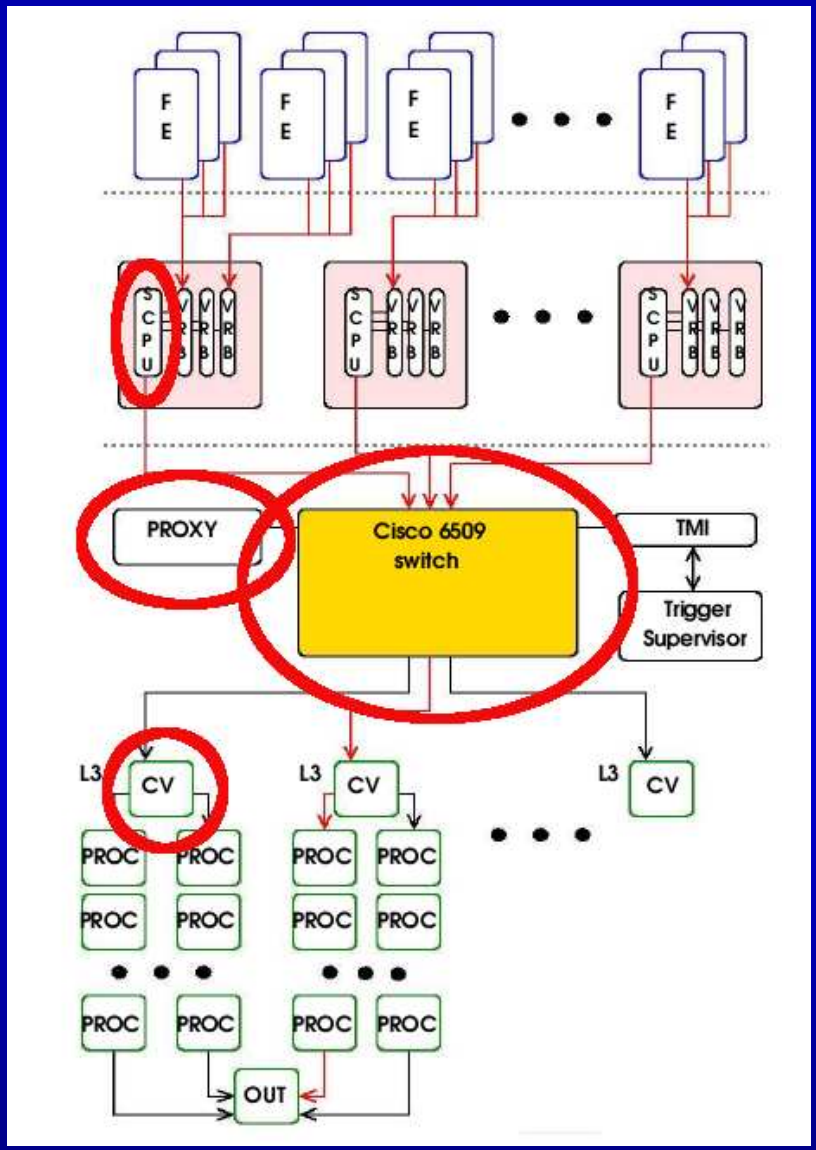
- Review of reason for balancing.
- Review of work done.
- Results of balancing.
- Status of EVB/L3 upgrade.
- What is left from Silicon End?

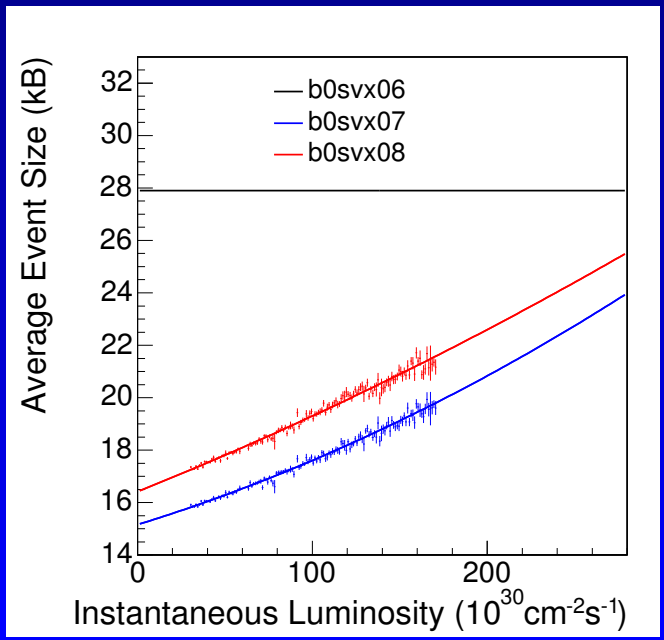
EVB/L3 Upgrade

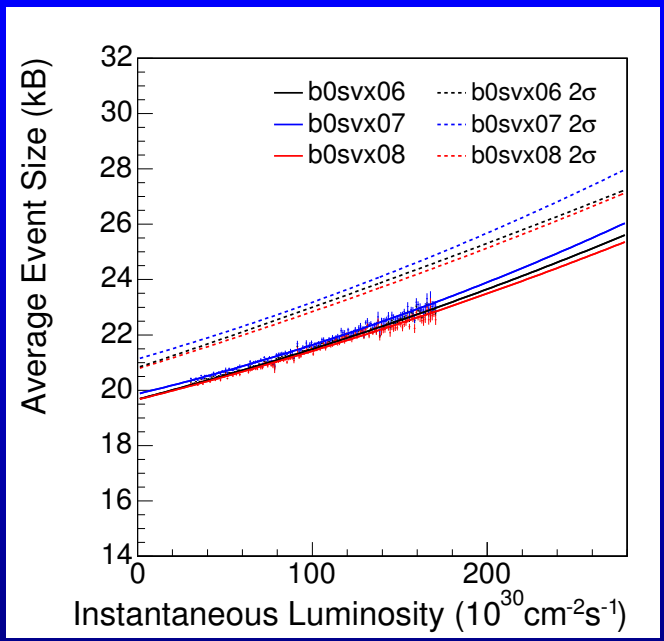
- The Run IIa EVB/L3 - design goal of 400 Hz L2A rate
- Old system limited by ATM switch that combined data from VRB crates
- EVB/L3 group carried out upgrade of system (upgraded components circled) with new design goal of 1000 Hz L2A rate (CDF Note 7327)
- End result - EVB/L3 system now limited by VME bus bandwidths of VRB crates, hence event size
- Non Silicon crates upgraded - L00 crate (b0svx06) became largest - we are bottleneck!



What did we do About it?

- Decided to balance events sizes of L00/ISL crate to minimize maximimum event sizes
- Need to change FIB to VRB connections, do virtually first
- Ran over DPHYSR stream looking at prescaled L2A
- Use strip info to create Ntuple with entries for event sizes per FIB and instantaneous luminosity
- Look at high luminosity stores from 10/2005-2/2006 (store 4634 right)
- Now able to look at event sizes for different balanced configurations in ntuple





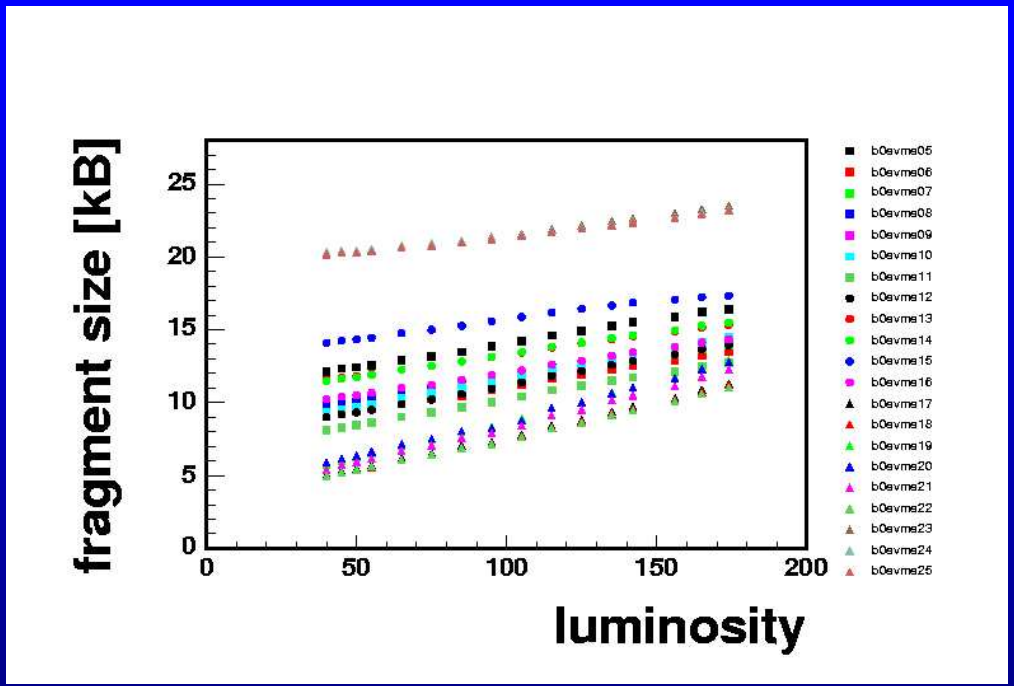
Choice of Balanced Configuration

- Chose configuration based on following criteria:
  - b0svx06/07/08 have balanced event sizes
  - Minimal changes from old configuration
  - Swap fibers at FIBs if possible (all except last entry below)

FIB Info			Old VRB Connection			New VRB Connection		
FIB	Crate	Slot	VRB	Crate	Slot	VRB	Crate	Slot
FIB_39	b0fib01	12	VRB_67	b0svx08	18	VRB_51	b0svx06	18
FIB_40	b0fib01	16	VRB_51	b0svx06	18	VRB_67	b0svx08	18
FIB_43	b0fib03	11	VRB_66	b0svx08	16	VRB_52	b0svx06	20
FIB_46	b0fib03	17	VRB_52	b0svx06	20	VRB_66	b0svx08	16
FIB_49	b0fib05	11	VRB_56	b0svx07	13	VRB_48	b0svx06	10
FIB_51	b0fib05	16	VRB_48	b0svx06	10	VRB_56	b0svx07	13
FIB_54	b0fib07	11	VRB_58	b0svx07	16	VRB_47	b0svx06	9
FIB_56	b0fib07	16	VRB_47	b0svx06	9	VRB_58	b0svx07	16
FIB_41	b0fib03	9	VRB_61	b0svx08	8	VRB_61	b0svx06	17

Did the Balancing Work?

- Yes, but...
- My tools for studying event size are currently broken, but Markus compiled plot below
- Top three overlapping points are the ISL/L00 VRB crates.
- Max size - 24 kBytes at inst. lumin. of 180E30, but approaching 28 kBytes with higher lumin.



Status of L3/EVB Upgrade

- Have run at 1150 Hz in 0 luminosity test.
- Have pushed system to 850 Hz in real data taking with 0 deadtime
- Waiting on trigger and ScalarMon changes to go faster
- Expect to run at $>$1 kHz with minimal deadtime at luminosities as high as 250E30
- Higher than that, ISL/L00 crates likely to be bottleneck

What's Left to Do

- Minor thing - Need to update FIB to VRB connections in CDF Note 6048
- Unfortunately, have not been able to find the source tex for the note
- Study threshold optimization in case we are bottleneck again
- Event size for threshold 9 (top right) vs. 11 (bottom right) for ISL
- For next shutdown, maybe add an additional VRB crate for ISL/L00